IN THE CLAIMS:

Please cancel claims 6-7 without prejudice or disclaimer, and amend claims 1 and 4 as follows:

1. (Currently Amended) A semiconductor integrated circuit device comprising:

first and second circuit blocks;

an interface checker which is ~~installed on~~ integrated into the semiconductor integrated circuit device so as to form one simulation model and which monitors whether waveforms of signals between the first and second circuit blocks conform to an interface specification of a design data of the first circuit block via the one simulation model; and

an external output pin which outputs ~~a result of a monitoring of the interface checker~~ outside of the semiconductor integrated circuit device a result of a monitoring of the interface checker.

2. (Original) The semiconductor integrated circuit device according to claim 1,

wherein the external output pin outputs a first value indicating a conformity of the waveforms to the interface specification or a second value indicating a nonconformity of the waveforms to the interface specification.

3. (Original) The semiconductor integrated circuit device according to claim 1,

wherein the interface specification describes timing information in synchronization with a clock signal.

4. (Currently Amended) A design method of a semiconductor integrated circuit device comprising:

providing a design data and an interface specification of the design data;

generating a synthesizable interface checker in accordance with the interface specification;

producing a semiconductor integrated circuit device including a first circuit block according to the design data and the interface checker according to the synthesizable interface checker, wherein the interface checker is integrated into the semiconductor integrated circuit device so as to form one simulation model; and

using the interface checker integrated into the semiconductor integrated circuit device via the one simulation model to monitor whether waveforms of signals between the first circuit block and another circuit block conform to the interface specification of the design data.

5. (Previously Presented) The design method of the semiconductor integrated circuit device according to claim 4, further comprising:

outputting a first value indicating a conformity of the waveforms to the interface specification or a second value indicating a nonconformity of the waveforms to the interface specification outside of the semiconductor integrated circuit device.

6-7. (Cancelled)